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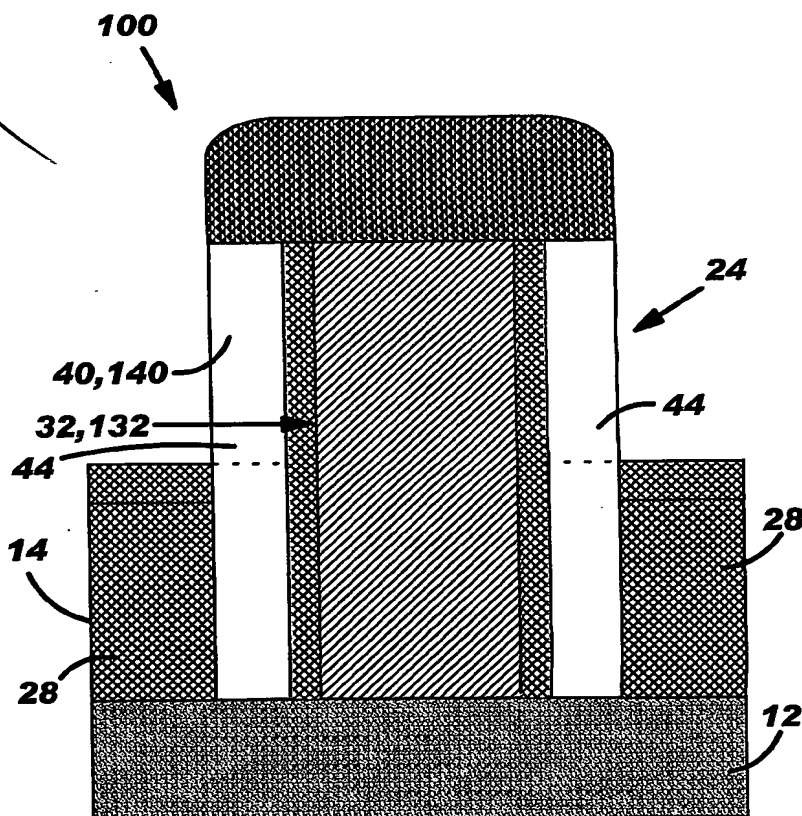
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**(54) Title:** METHODS OF FORMING STRUCTURE AND SPACER AND RELATED FINFET



**(57) Abstract:** Methods for forming a spacer (44) for a first structure (24, 124), such as a gate structure of a FinFET, and at most a portion of a second structure (14), such as a fin, without detrimentally altering the second structure. The methods generate a first structure (24) having a top portion (30, 130) that overhangs an electrically conductive lower portion (32, 132) and a spacer (44) under the overhang (40, 140). The overhang (40, 140) may be removed after spacer processing. Relative to a FinFET, the overhang protects parts of the fin (14) such as regions adjacent and under the gate structure (24, 124), and allows for exposing sidewalls of the fin (14) to other processing such as selective silicon growth and implantation. As a result, the methods allow sizing of the fin (14) and construction of the gate structure (24, 124) and spacer without detrimentally altering (e.g., eroding by forming a spacer thereon) the fin (14) during spacer processing. A FinFET (100) including a gate structure (24, 124) and spacer (44) is also disclosed.

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